100 V, 2.0 A, Low $V_{CE(sat)}$ NPN Transistor
NSS1C201MZ4, NSV1C201MZ4

onsemi's e^2PowerEdge family of low $V_{CE(sat)}$ transistors are miniature surface mount devices featuring ultra low saturation voltage ($V_{CE(sat)}$) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical applications are DC−DC converters and power management in portable and battery powered products such as cellular and cordless phones, PDAs, computers, printers, digital cameras and MP3 players. Other applications are low voltage motor controls in mass storage products such as disc drives and tape drives. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e^2PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

Features

- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V_{CEO}	100	Vdc
Collector-Base Voltage	V_{CBO}	140	Vdc
Emitter-Base Voltage	V_{EBO}	7.0	Vdc
Collector Current − Continuous	I_C	2.0	A
Collector Current − Peak	I_{CM}	3.0	A

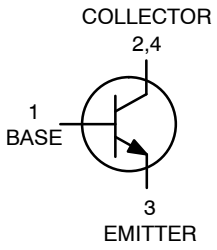
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D (Note 1)	 800 6.5	 mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$ (Note 1)	155	°C/W
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D (Note 2)	 2.0 15.6	 W mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$ (Note 2)	64	°C/W
Total Device Dissipation (Single Pulse < 10 sec.)	$P_{Dsingle}$ (Note 3)	710	mW
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. FR−4 @ 7.6 mm^2, 1 oz. copper traces.
2. FR−4 @ 645 mm^2, 1 oz. copper traces.
3. Thermal response.

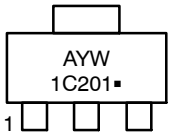
100 VOLTS, 2.0 AMPS NPN LOW $V_{CE(sat)}$ TRANSISTOR



MARKING DIAGRAM

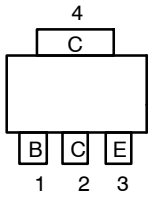


SOT−223
CASE 318E
STYLE 1



A	= Assembly Location
Y	= Year
W	= Work Week
1C201	= Specific Device Code
▪	= Pb−Free Package

PIN ASSIGNMENT



Top View Pinout

ORDERING INFORMATION

Device	Package	Shipping†
NSS1C201MZ4T1G NSV1C201MZ4T1G	SOT−223 (Pb−Free)	1000/ Tape & Reel
NSS1C201MZ4T3G	SOT−223 (Pb−Free)	4000/ Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector – Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	100			Vdc
Collector – Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	140			Vdc
Emitter – Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	7.0			Vdc
Collector Cutoff Current (V_{CB} = 140 Vdc, I_E = 0)	I_{CBO}			100	nA
Emitter Cutoff Current (V_{EB} = 6.0 Vdc)	I_{EBO}			50	nA
ON CHARACTERISTICS					
DC Current Gain (Note 4) (I_C = 10 mA, V_{CE} = 2.0 V) (I_C = 500 mA, V_{CE} = 2.0 V) (I_C = 1.0 A, V_{CE} = 2.0 V) (I_C = 2.0 A, V_{CE} = 2.0 V)	h_{FE}	 150 120 80 40		 360	
Collector – Emitter Saturation Voltage (Note 4) (I_C = 0.1 A, I_B = 0.010 A) (I_C = 0.5 A, I_B = 0.050 A) (I_C = 1.0 A, I_B = 0.100 A) (I_C = 2.0 A, I_B = 0.200 A)	$V_{CE(sat)}$			 0.030 0.060 0.100 0.180	V
Base – Emitter Saturation Voltage (Note 4) (I_C = 1.0 A, I_B = 0.100 A)	$V_{BE(sat)}$			 1.10	V
Base – Emitter Turn–on Voltage (Note 4) (I_C = 1.0 A, V_{CE} = 2.0 V)	$V_{BE(on)}$			0.850	V
Cutoff Frequency (I_C = 100 mA, V_{CE} = 5.0 V, f = 100 MHz)	f_T		100		MHz
Input Capacitance (V_{EB} = 0.5 V, f = 1.0 MHz)	Cibo		305		pF
Output Capacitance (V_{CB} = 3.0 V, f = 1.0 MHz)	Cobo		22		pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulsed Condition: Pulse Width = 300 msec, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

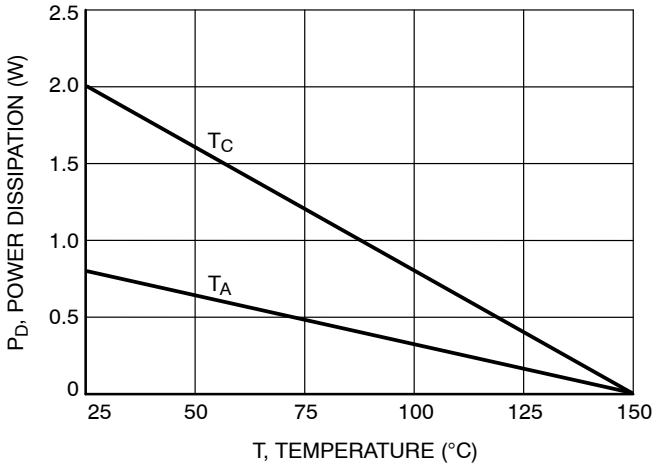


Figure 1. Power Derating

TYPICAL CHARACTERISTICS

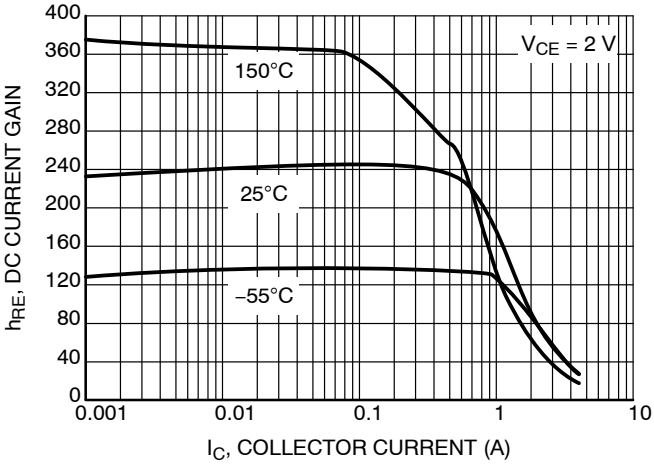


Figure 2. DC Current Gain

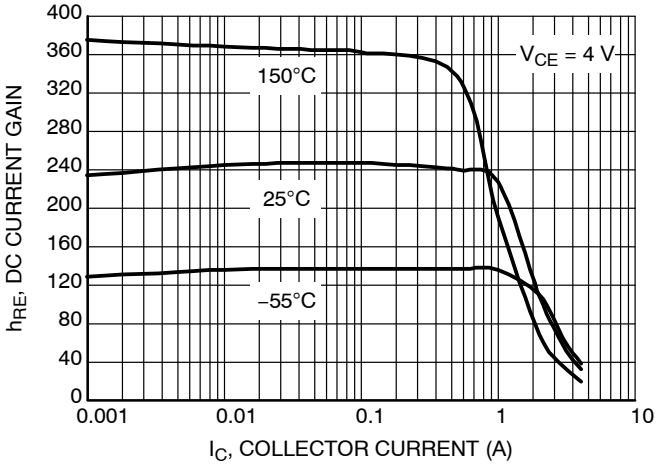


Figure 3. DC Current Gain

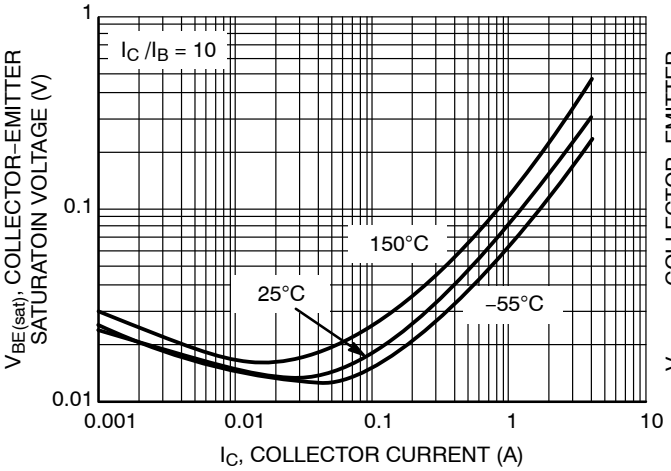


Figure 4. Collector−Emitter Saturation Voltage

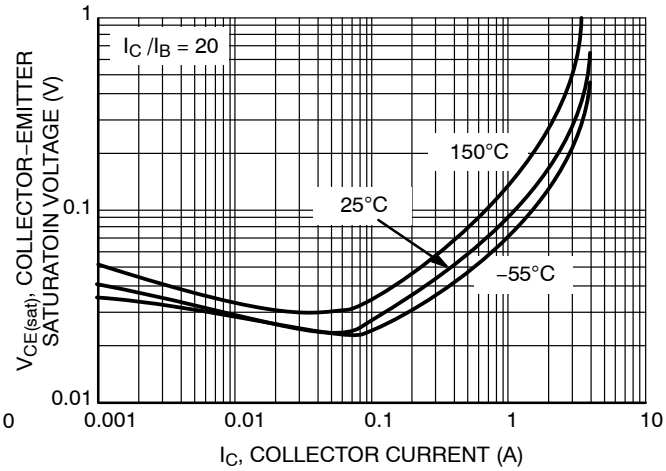


Figure 5. Collector−Emitter Saturation Voltage

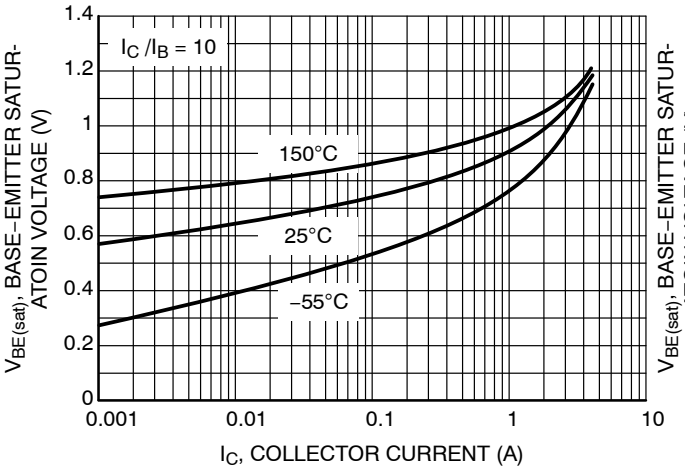


Figure 6. Base−Emitter Saturation Voltage

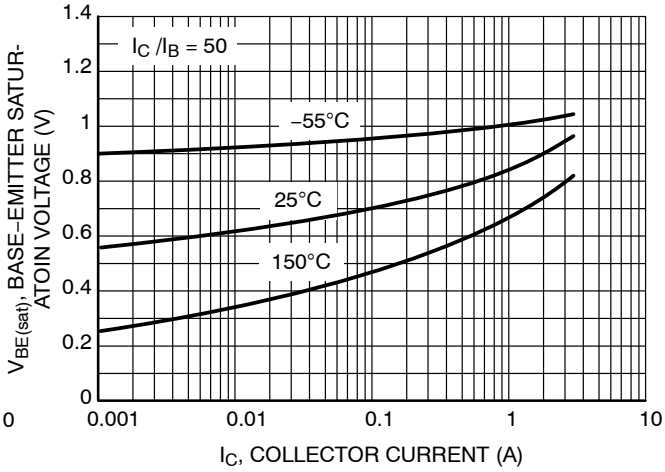


Figure 7. Base−Emitter Saturation Voltage

TYPICAL CHARACTERISTICS

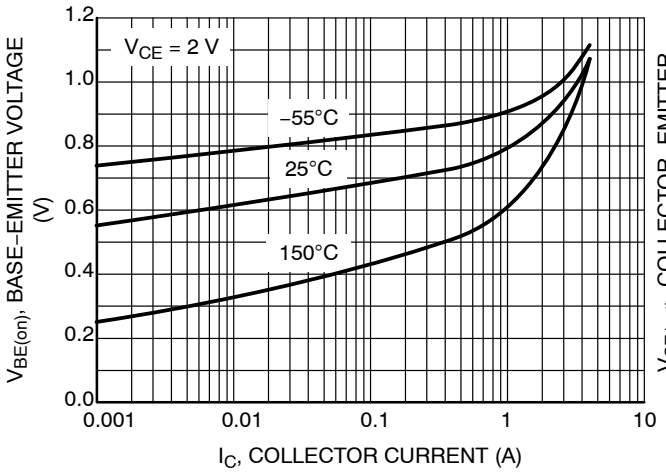


Figure 8. Base−Emitter Voltage

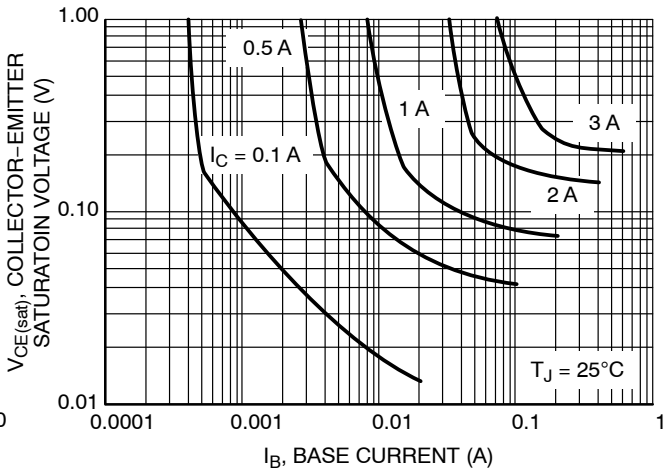


Figure 9. Collector Saturation Region

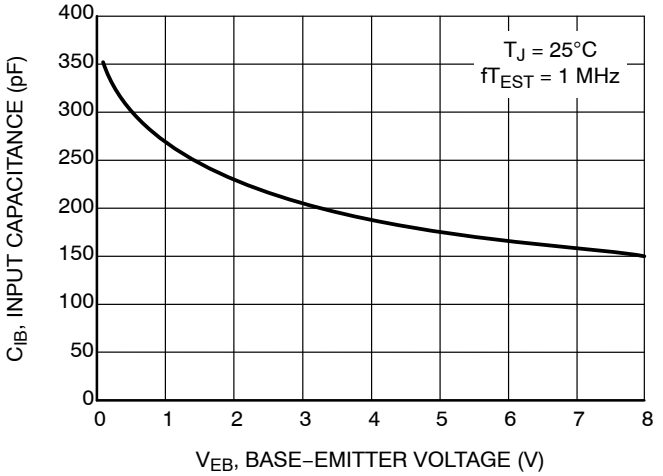


Figure 10. Input Capacitance

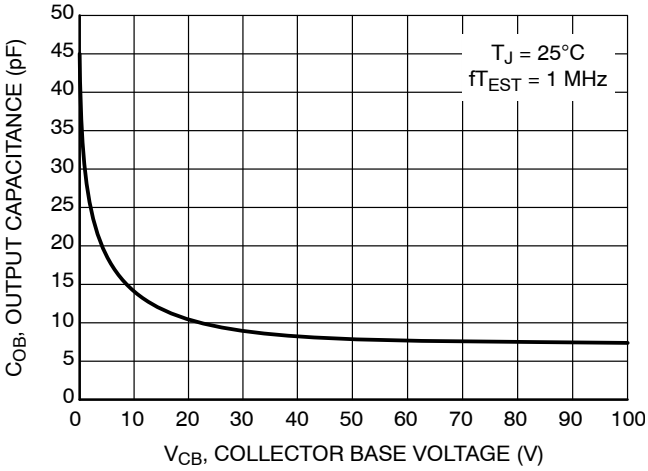


Figure 11. Output Capacitance

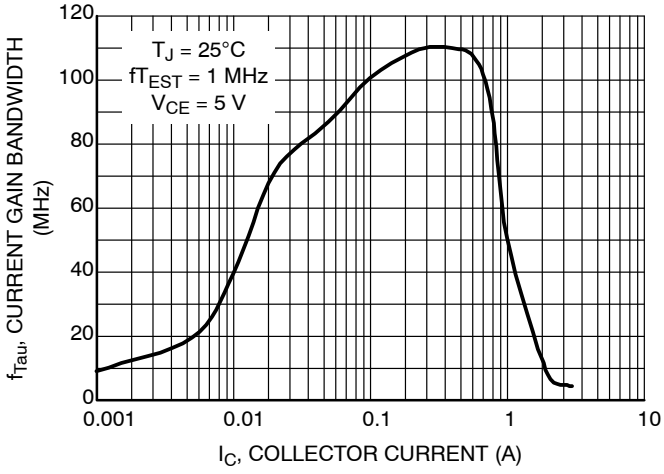


Figure 12. Current Gain Bandwidth Product

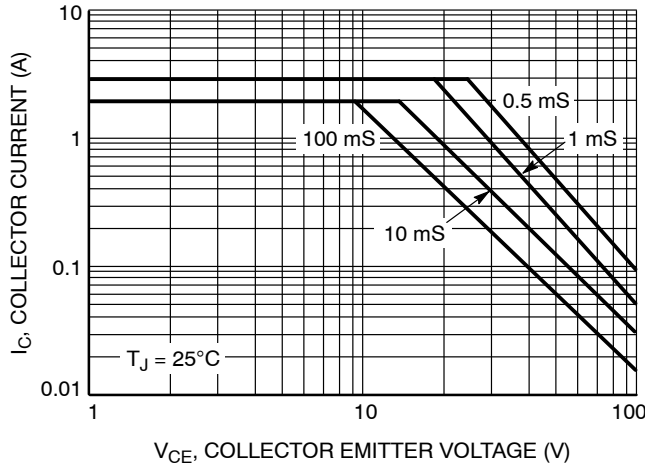


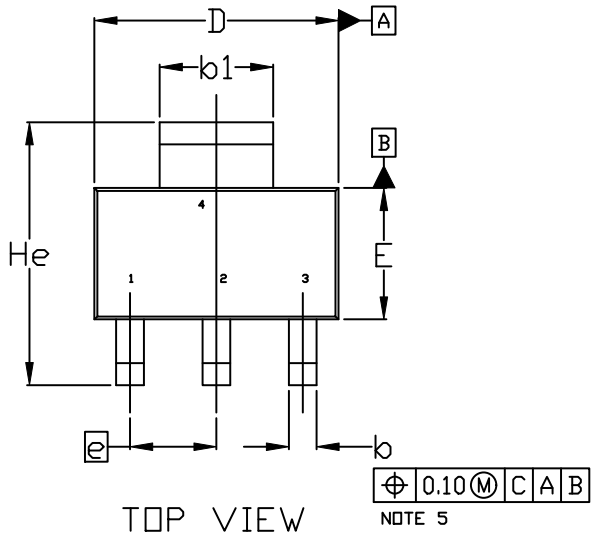
Figure 13. Safe Operating Area

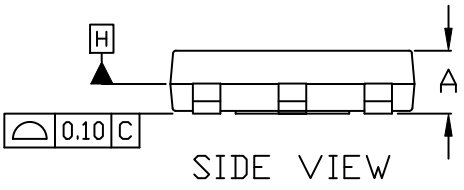


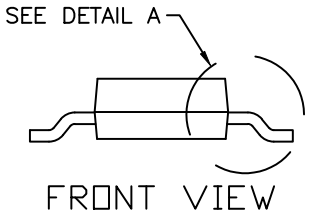
SCALE 1:1

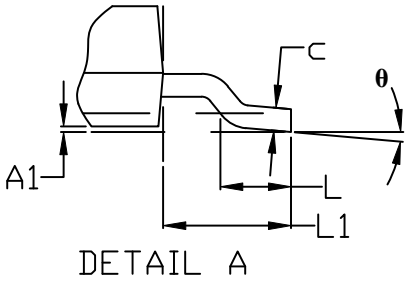
SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018



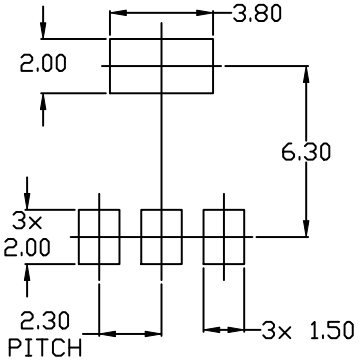






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



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SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

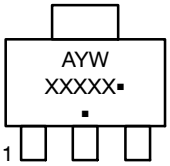
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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